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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,591	05/19/2005	Jan-Willem Van De Waerd	US02 0465 US	7635
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NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER CYGIEL, GARY W	
			ART UNIT 2187	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/535,591

Applicant(s)

VAN DE WAERDT ET AL.

Examiner

Gary W. Cygiel

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/CD)
Paper No(s)/Mail Date 5/11/2010
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06 May 2010 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-8, 10-14, 16-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood).

Consider **Claim 1**,

Sherwood teaches a method of data retrieval comprising the steps of:

providing a first memory circuit (Sherwood:Fig 3);

providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

providing cache memory circuit (Sherwood:Fig 3);

executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

only allowing accesses to the SPT in response to a detection of a cache miss (Sherwood:Sec 4.2/4.3, the load-PC (for a missed load) is used to index into the stride table.);and

only allowing updates to the SPT in response to the detection of a cache miss. (Sherwood:Sec 4.2/4.3, prediction table is only updated on a cache miss (Sec 4.2 ¶2)).

Consider **Claims 2 and 16**,

Sherwood further teaches wherein the cache memory circuit is a stream buffer (Sherwood:Fig 3).

Consider **Claim 4**,

Sherwood further teaches wherein the cache memory circuit and the SPT are within a same physical memory space (Sherwood:Fig 3).

Consider **Claim 5**,

Sherwood further teaches wherein the first memory is an external memory circuit separate from a processor executing the instructions (Sherwood:Fig 3,data line from/to next lower level of memory.).

Consider **Claims 6 and 7**,

Sherwood further teaches wherein the step of detecting a cache miss includes the steps of:

determining whether an instruction to be executed by the processor is a memory access instruction;

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and,

when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred (Sherwood:Sec 4.3 ¶3, a cache miss occurs when a requested memory line is not in the cache, therefore requiring the first two limitations of these claims.).

Consider **Claim 8**,

Sherwood further teaches wherein the step of allowing access provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.3).

Consider **Claim 10**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Consider **Claim 11**,

Sherwood teaches an apparatus comprising:

a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.); and

a filter circuit for use with the SPT, the filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected (Sherwood:Sec 4.2/4.3, the load-PC (for a missed load) is used to index into the stride table; prediction table is only updated on a cache miss (Sec 4.2 ¶2.).

Consider **Claim 12**,

Sherwood further teaches a memory circuit, the memory circuit for storing the SPT therein (Sherwood:Fig 3).

Consider **Claim 13**,

Sherwood further teaches a cache memory, the cache memory residing within the memory circuit (Sherwood:Fig 3).

Consider **Claim 14**,

Sherwood further teaches wherein the memory circuit is a single ported memory circuit (Sherwood:Fig 3, Page 5, paragraph labeled prediction, only one request can be processed at a time.)

Consider **Claim 17**,

Sherwood teaches a method of data retrieval comprising the steps of:

- providing a first memory circuit (Sherwood:Fig 3);

- providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

- providing cache memory circuit (Sherwood:Fig 3);

- executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

- detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

- restricting accesses to the SPT in response to the detection of a cache miss (Sherwood:Sec 4.2/4.3; the load-PC (for a missed load) is used to index into the stride table, prediction table is only updated on a cache miss (Sec 4.2 ¶2)).

Consider **Claim 18**,

Sherwood further teaches wherein the step of restricting provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.2/4.3).

Consider **Claim 20**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
6. Claims 3, 9, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood) in view of Handy (NPL: the Cache Memory book) (hereinafter referred to as Handy).

Consider **Claim 3, 9, 15 and 19**,

Sherwood teaches a method according to claim 1 or 13 respectively, but does not specifically disclose all the details regarding the circuits construction.

Handy does teach these limitations such as:

wherein the cache memory circuit is a random access cache memory (Handy:Page 28, SRAM cell used in internal cache.).

wherein the cache memory circuit is integral with the processor executing the instructions (Handy:Page 28, CPU on same chip as on-chip cache.).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the circuit construction concepts as taught by Handy in the system of Sherwood because they are notoriously well known concepts in the art. The use of these methods constitutes only design choice and has no novelty in the art.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood) in view of Matas et al. (NPL:Memory 1997).

Consider **Claim 21**,

Sherwood teaches a method of data retrieval, the method comprising:

providing a first memory circuit (Sherwood:Figure 3);

providing a memory having a cache memory circuit and a stride prediction table (Sherwood:Figure 3) that is indexed with cache line miss information (Sherwood:Fig 3, Sec. 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3, only cache block addresses are used);

in a filter circuit,

receiving an application stream having a plurality of access instructions for accessing data in the first memory circuit (Sherwood:Page 8, Table 2; Page 9:Left Column, describes various programs (application streams)).

for each of the plurality of access instructions that are load access instructions,

accessing the cache memory to determine whether data at a memory location of the load access instruction is present within the cache (Sherwood:Page 5:section 4.2, determining if instruction hit or missed in cache.), and

when the data is other than present within the cache, detecting a cache miss for the load access instruction (Sherwood:Page 6:Sec. 4.3, detects two cache misses in a row.),

restricting accesses and updates to the SPT to only load memory access instructions for which a cache miss is detected (Sherwood:Sections 4.2/4.3, load-PC

(for a missed load) is used to index into the stride table; prediction table is only updated on a cache miss (Sec 4.2 ¶(2).);

in response to an update to the SPT indicative of one of said detected cache misses, executing instructions to access the SPT and predict a cache miss (Sherwood:Section 4.3, allocates a stream buffer in response to two cache misses. Sec 3.3.2 describes stream buffer operation.); and

in response to a predicted cache miss, control the loading of a stream cache based upon the memory location of the load access instruction (Sherwood:Sections 4.2/4.3, stride based buffer allocation. Sec 3.3.2 describes stream buffer operation.).

Sherwood fails to expressly describe the use of a single-ported SRAM for the cache memory circuit and stride prediction table. However, Matas et al. does describe the use of SRAM for cache memory applications. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use single-port SRAM (Matas:Fig. 8-6/8-7) for the cache memory circuit and stride prediction table of Sherwood because single-port SRAM is commonly used in cache applications and is faster and uses less power than other types of memories (Matas:Page 8-1 ¶(1)).

Response to Arguments

1. Applicant's arguments filed 11 May 2010 have been fully considered but they are not persuasive.

[A] Re: SPT is accessed independent of a cache miss.

The applicant argues that the SPT is accessed during events other than a cache miss. The applicant uses Figure 2 and description from section 4.1 in support of this assertion. The examiner notes that Figure 2 and Figure 3 are different. Figure 3 shows that the only input into the stride table comes from the write back stage when the load-PC is used to index into the stride table (Sherwood:Sec. 4.2 ¶3).

The applicant states (Page 7) that "no portion of the cited sections 4.2 and 4.3 discloses updating a stride table only on a cache miss." However, Sherwood explicitly describes (Sherwood:Sec 4.2 ¶2) that "the prediction table is **only** updated on a miss" [Emphasis Added].

The applicant also alleges (Page 7) that the description from Sec. 4.2 on Page 5 states that "the stride table includes both a last and a current address." The examiner has reviewed Section 4.2 and finds no mention of a current address being stored in the stride table. Sherwood describes that the stride table stores "(1) the last address for the load, (2) the last stride for the load, (3) the 2-delta stride, and (4) some confidence information." There is no mention of storing a current address in the stride table.

[B] Re: Claims 6 and 7

The applicant argues that the following steps of Claims 6 and 7 are not necessarily present in the Sherwood reference:

determining whether an instruction to be executed by the processor is a memory access instruction; and

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache.

Sherwood describes that "In the write-back stage, the load instruction is checked to see if it hit or missed in the L1 data cache." This requires determining whether data at a memory location of the memory access instruction is present within the cache. An attempt to access the cache is the result of determining that an instruction to be executed by the processor is a memory access instruction.

The applicant argues that there may be other ways to detect a cache miss, but fails to provide an example of how this can be accomplished without some determination that the instruction is a memory access instruction and further determining whether the data is in the cache. Cache miss information cannot "simply be provided" or provided "based upon functionality that happens after a cache miss" without the above steps because without the above steps cache miss information simply does not exist.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary W. Cygiel whose telephone number is (571)270-1170. The examiner can normally be reached on Tuesdays and Thursdays 12:00pm-2:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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